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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/843,533	04/25/2001	William Fornaciari	851763.406	7410

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EXAMINER	
HUYNH, KIM T	
ART UNIT	**PAPER NUMBER**
2112	

DATE MAILED: 11/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/843,533	FORNACIARI ET AL.	
	Examiner	Art Unit	
	Kim T. Huynh	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,4,6,15-22 and 24-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,6,15-22 and 24-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3-4, 6, 15-22, 24-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Martwick (US Patent 6,336,158) in view of Ramprasad (IEEE transactions on very large scale integration (VLSI) systems, vol.7, No. 2, June 1999, page 212-221)

As per claims 1, 15, 22, 25, 29, 37, Martwick discloses a circuit architecture for buses, comprising: encoder/decoder architecture for buses, capable of receiving a current value of input information relating to a given instant and of generating, from this current input value, a corresponding output value relating to the same given instant on encoded bus lines, the encoder/decoder architecture comprising: (col.7, lines 6-23)

- At least one memory element for storing the respective preceding input information value and output information value, (col.8, line 55-col.9, line 28)
- A prediction block for generating an estimate of the current input information value on the basis of the preceding input information value, and (col.7, lines 5-23), (col.8, line 55-col.9, line 28)

- A decorrelation block for decorrelating the current input information value with respect to the estimate, to produce a decorrelation result, (col.5, lines 37-67)
- The current output value adapted to be selected as one of the following:
    - The current input information value, (col.8, line 55-col.9, line 12)
    - The preceding output value, and (col.8, line 55-col.9, line 12)
    - The decorrelation result. (col.8, line 55-col.9, line 12)

Martwick discloses all the limitations as above except the a redundant line, preferably configured to transfer information on the sequentiality of the information, acting as a prediction block, an XOR logic gate, acting as a decorelation block, and a multiplexer, acting as a selection block, and a multiplexer, acting as a selection block for selecting the current output value. However, Ramprasad discloses data transfers on microprossor address busses are often sequential (i. E., current data value equals the previous data equals the previous data value plus a constant increment) due to fetches of instructions and array elements; (page 212, col.2, paragraph 2nd); furthermore, Ramprasad discloses XOR gate to generate the corresponding signal waveforms on the bus and its function is given by a bit-wise exclusive-or of the current input and the prediction, the encoder/decoder employing control line into a multiplexer that selects outputs depending on whether the input is to be encoded or

decoded, respectively. (page 214, col.2, paragraph 4-page 215, col.1, paragraph 2)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Ramprasad's teaching into Martwick's system so as to reduce transition activity. (abstract)

As per claim 3, Martwick discloses wherein the at least one memory element comprises corresponding registers for storing the corresponding preceding input information values and output information values. (col. 6, lines 13-51)

As per claim 4, martwick discloses wherein at least one of the blocks is at least partially implemented by means of pass-gates. (col.9, lines 13-29)

As per claim 16, Martwick discloses wherein the at least one bus interface operates at sub-system level. (col.5, lines 2-37)

As per claim 17, Martwick discloses wherein the at least one bus interface operates at the processor-to-cache bus level. (col.3, lines 58-65), (col.6, lines 31-51)

As per claim 18, Martwick discloses wherein the at least one bus interface operates at system level. (col.4, line 48-col.5, 20)

As per claim 19, Martwick discloses configured in the form of a shared memory multiprocessor system. (col.3, lines 47-65)

As per claim 20, Martwick discloses all the limitations as above except fails to disclose the system comprising a structure of the monolithic type.

Examiner takes official notice that monolithic type structure of the system are well known in the art. It would have been obvious one having ordinary skills in the art at the time the invention was made to include monolithic type to form single type of substrate material so as to be compatible in the multichip system.

As per claim 21, Martwick discloses the system comprising a structure of the multichip type. (fig.1, wherein each block may integrated a single chip, many block formed multichip type)

As per claims 24, 31, 32, Martwick discloses a bus interface for a bus comprising:

- An input for receiving a current input information value; (col.8, line 55-col.9, line 12)
- At least one register coupled to the input to receive and store a respective preceding input information value and coupled to an output to store a preceding output value; (col.8, line 55-col.9, line 28)
- A prediction block coupled to the registers and configured to generate an estimate of the current input information value based on the preceding input information value; (col.7, lines 5-23), (col.8, line 55-col.9, line 28)
- A decorrelation block coupled to the input and the prediction block and configured to decorrelate the current input information value with respect to the estimate and to generate a decorrelation result; and (col.5, lines 37-67)

- A selection block coupled to the input and the decorrelation block and configured to select and a current output value from one of the current input information value, the decorrelation result, and the preceding output value; (col.8, line 55-col.9, line 12)
- Wherein the prediction module comprises an identify module; (col.5,lines 38-67)

Martwick discloses all the limitations as above except the decorrelation block comprises an XOR logic gate; and the selection block comprises an inverter configured to select the current output value. However, Ramprasad discloses XOR gate to generate the corresponding signal waveforms on the bus and its function is given by a bit-wise exclusive-or of the current input and the prediction, the encoder/decoder employing control line into a multiplexer that selects outputs depending on whether the input is to be encoded or decoded, respectively. (page 214, col.2, paragraph 4-page 215, col.1, paragraph 2). In addition, Ramprasad discloses the difference-based mapping function returns the difference and properly adjusted so that the output fits, which it is require inverters, multiplexers each at encoder/decoder for implementing the outputs. (pape 215, col.1, paragraph 1)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Ramprasad's teaching into Martwick's system so as to reduce transition activity. (abstract)

As per claims 26, 28, 30, 33, 38, Martwick discloses a bus interface for a bus, comprising:

- An input for receiving a current input information value; (col.8, line 55-col.9, line 12)
- At least one register coupled to the input to receive and store a respective preceding input information value and coupled to an output to sore a preceding output value; (col.8, line 55-col.9, line 28)
- A prediction block coupled to the registers and configured to generate an estimate of the current input information value based on the preceding input information value; (col.7, lines 5-23), (col.8, line 55-col.9, line 28)
- A decorrelation block coupled to the input and the prediction block and configured to decorrelate the current input information value with respect to the estimate and to generate a decorrelation result; and (col.5, lines 37-67)
- A selection block coupled to the input and the decorrelation block and configured to select a current output value from one of the current input information value, the decorrelation result, and the preceding output value; (col.8, line 55-col.9, line 12)

Martwick discloses all the limitations as above except wherein the prediction block comprises a redundant line configured for transferring information on the sequentiality of the received input information value; the decorrelation block comprising an XOR logic gate; and the selection block

comprising an XOR logic gate configured to select the current output value. However, Ramprasad discloses data transfers on microprossor address busses are often sequential (i. E., current data value equals the previous data equals the previous data value plus a constant increment) due to fetches of instructions and array elements; (page 212, col.2, paragraph 2nd); furthermore, Ramprasad discloses XOR gate to generate the corresponding signal waveforms on the bus and its function is given by a bit-wise exclusive-or of the current input and the prediction, the encoder/decoder employing control line into a multiplexer that selects outputs depending on whether the input is to be encoded or decoded, respectively. (page 214, col.2, paragraph 4-page 215, col.1, paragraph 2)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Ramprasad's teaching into Martwick's system so as to reduce transition activity. (abstract)

As per claims 27, 35, Martwick discloses a bus interface for a bus, comprising:

- An input for receiving a current input information value; (col.8, line 55-col.9, line 12)
- At least one register coupled to the input to receive and store a respective preceding input information value and coupled to an output to sore a preceding output value; (col.8, line 55-col.9, line 28)
- A prediction block coupled to the registers and configured to generate an estimate of the current input information value based on the preceding input information value; (col.7, lines 5-23), (col.8, line 55-col.9, line 28)

- A decorrelation block coupled to the input and the prediction block and configured to decorrelate the current input information value with respect to the estimate and to generate a decorrelation result; and (col.5, lines 37-67)
- A selection block coupled to the input and the decorrelation block and configured to select a current output value from one of the current input information value, the decorrelation result, and the preceding output value; (col.8, line 55-col.9, line 12)
- wherein the prediction block comprises an identity module, and the decorrelation block comprises a difference module configured to also select the current output value. (col.8, line 55-col.9, line 12), (col.5, lines 37-67)

As per claim 34, Martwick discloses a circuit architecture for buses, comprising: encoder/decoder architecture for buses, capable of receiving a current value of input information relating to a given instant and of generating, from this current input value, a corresponding output value relating to the same given instant on encoded bus lines, the encoder/decoder architecture comprising: (col.7, lines 6-23)

- At least one memory element for storing the respective preceding input information value and output information value, (col.8, line 55-col.9, line 28)

- A prediction block for generating an estimate of the current input information value on the basis of the preceding input information value, and (col.7, lines 5-23), (col.8, line 55-col.9, line 28)
- A decorrelation block for decorrelating the current input information value with respect to the estimate, to produce a decorrelation result, (col.5, lines 37-67)
- The current output value adapted to be selected as one of the following:
    - The current input information value, (col.8, line 55-col.9, line 12)
    - The preceding output value, and (col.8, line 55-col.9, line 12)
    - The decorrelation result. (col.8, line 55-col.9, line 12)

Martwick discloses all the limitations as above except wherein the selection block comprises an inverter and a pass-gate. However, Ramprasad discloses XOR gate to generate the corresponding signal waveforms on the bus and its function is given by a bit-wise exclusive-or of the current input and the prediction, the encoder/decoder employing control line into a multiplexer(pass-gate) that selects outputs depending on whether the input is to be encoded or decoded, respectively. (page 214, col.2, paragraph 4-page 215, col.1, paragraph 2)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Ramprasad's teaching into Martwick's system so as to reduce transition activity. (abstract)

As per claim 36, Martwick discloses a circuit architecture for buses, comprising: encoder/decoder architecture for buses, capable of receiving a current value of input information relating to a given instant and of generating, from this current input value, a corresponding output value relating to the same given instant on encoded bus lines, the encoder/decoder architecture comprising: (col.7, lines 6-23)

- At least one memory element for storing the respective preceding input information value and output information value, (col.8, line 55-col.9, line 28)
- A prediction block for generating an estimate of the current input information value on the basis of the preceding input information value, and (col.7, lines 5-23), (col.8, line 55-col.9, line 28)
- A decorrelation block for decorrelating the current input information value with respect to the estimate, to produce a decorrelation result, (col.5, lines 37-67)
- The current output value adapted to be selected as one of the following:
    - The current input information value, (col.8, line 55-col.9, line 12)
    - The preceding output value, and (col.8, line 55-col.9, line 12)
    - The decorrelation result. (col.8, line 55-col.9, line 12)
    - An identity module, acting as a prediction module, and (col.8, line 55-col.9, line 12), (col.5, lines 37-67)

- A difference module, acting as a decorrelation block, and(col.8, line 55-col.9, line 12), (col.5, lines 37-67)

Martwick discloses all the limitations as above except an XOR logic gate, acting as a selection block capable of selecting the said current output value. However, Ramprasad discloses XOR gate to generate the corresponding signal waveforms on the bus and its function is given by a bit-wise exclusive-or of the current input and the prediction, the encoder/decoder employing control line into a multiplexer that selects outputs depending on whether the input is to be encoded or decoded, respectively. (page 214, col.2, paragraph 4-page 215, col.1, paragraph 2)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Ramprasad's teaching into Martwick's system so as to reduce transition activity. (abstract)

Response to Amendment

3. Applicant's amendment filed on 8/17/04 have been fully considered but does not place the application in condition for allowance.

a. In response to applicant's argument that Martwick does not teach or suggest the use of a prediction block, a decorrelation block and at least one register for selecting one from among current input information value, a decorrelation result, and a preceding output value. Examiner respectfully disagrees. As Martwick notes at col.7, lines 15-col.9, line 29), discloses upon receipt address, the I/O controller checks to see whether

information corresponding to the received transaction address is already contained in the I/O map. The I/O controller then proceeds to snoop the I/O decode map with the present transaction address, to retrieve relevant decode information. The processing block 206 determining whether the I/O decode map information indicates that a transaction address is owned. In order to determine ownership, the I/O controller approach to access decode bit information stored within the I/O map. Data output transaction address are respectively compared for a match within the comparator. If a match is found an appropriate logical level output is output from the comparator. Thus, the prior art teaches the invention as claimed and the claims do not distinguish over the prior art as applied, therefore it is properly stated in the rejection of record.

b. In response to applicant's argument that Ramprasad teach circuit being adapted to be implemented as a single, respective encoding scheme. This is contrary to the present invention, which is configured to select one from among current information values, preceding output values, and a decorrelation result. Examiner respectfully disagrees. As Ramprasad notes on page 214-215 started from last paragraph of page 214, The hardware between the encoder and decoder in a bidirectioonal pad can be shared by control line into a multiplexer or (Xor) that selects the output depending on the inputs. Thus, the prior art teaches the invention as claimed and the claims do not distinguish over the prior art as applied, therefore it is properly stated in the rejection of record.

Conclusion

4. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (571)272-3635 or via e-mail addressed to [kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 9.00AM- 6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (571)272-3632 or via e-mail addressed to [mark.rinehart@uspto.gov]. The fax phone numbers for the organization where this application or proceeding is assigned are (703)872-9306 for regular communications and After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-2100.

Kim Huynh

November 11, 2004

TIMVO
PRIMARY EXAMINER